ISSN 2349-7815

International Journal of Recent Research in Electrical and Electronics Engineering (IJRREEE)
Vol. 4, Issue 2, pp: (110-116), Month: April - June 2017, Available at: www.paperpublications.org

A Soft Switched Dual Buck Inverter with Series Connected Diodes and Single Inductor

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Abstract: **In an inversion system, high reliability is one of the main targets pursuing. Some problems will threaten the reliability of the system, such as, the shoot through issue and the failure of reverse recovery. The dual buck inverters can solve the above problems without adding dead time. A new topology of dual buck inverter with series connected diodes and a single inductor is presented here. The system retains the advantage of no reverse recovery of body diode. The inverter has just one filter inductor, which can make the volume and weight of the system decreased observably and improve the integration. By providing soft switching techniques the power loss can be well reduced. A resonant circuit contributes to reduced switching loss by providing ZVS property. The whole system is simulated in PSIM environment. This inverter retains the advantage of high reliability. A PIC microcontroller is used to generate control pulses since it is fast and easy to implement program when we compare with other microcontrollers. The ease of programming and interfacing with other peripherals make PIC a successful microcontroller. A two level inverter output can be well verified at the output of the dual buck inverter without any reverse recovery loss.**

Keywords: **Body diode, PSIM, Reverse recovery, Soft Switching, SPWM, ZCS, ZVS.**

I. INTRODUCTION

The fast development of the clean energy power generation requires the inversion system, especially the inverters, to be more and more reliable. Yet shoot through problem of the power devices is a major threaten to the reliability. As is known, a traditional method to solve the shoot through issue is by setting dead time. However, the dead time will cause a distortion of the output current. Also, during the dead time, the current may flow through the body diode of the switch which can cause the failure of the reverse recovery [1]. For the purpose of solving the above problems, the dual buck topologies are proposed in a lot of research. By combining two unidirectional buck circuits, the dual buck inverters will not suffer threaten of shoot through problem and the freewheeling current will flow through the independent diodes which can solve the reverse recovery problem of the MOSFET's body diodes. However, the major drawback of the dual buck topologies is the magnetic utilization. Only half of the inductance is used in every working mode. And it will obviously increase the weight and volume of the system [2],[4]. This project presents a kind of novel phase leg topology with series connected diodes and single inductor to highly improve the reliability of the inverter, especially for the MOSFET inverter [6]. Applying the phase leg to the single phase inverter, an improved single inductor dual buck inverters are proposed in this paper. The novel topology has the following advantages. Firstly, retains the advantages of the traditional dual buck inverters, secondly, makes full use of the inductance, thirdly, the proposed inverter saves two switches compared to the traditional single inductor topology, which makes a lower conducting loss and a simpler controlling strategy. The simulation and experimental results have verified using PSIM.

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The expression "soft switching" actually refers to the operation of power electronic switches as zero-voltage switches (ZVS) or zero-current switches (ZCS). Present day, fast converters operate at much higher switching frequencies chiey to reduce weight and size of the filter components. As a consequence, switching losses now tend to pre- dominate, causing the junction temperatures to rise. Special techniques are employed to obtain clean turn-on and turn-off the devices. By introducing an auxiliary circuit to the dual buck inverter, an improved inverter with no shoot through issue as well as reduced switching loss can be ensured. Comparing with other dual buck inverters, the proposed inverter can also increase the input voltage utilization rate and reduce the voltage stress by the voltage commutation bridge. Moreover, the inverter just needs one inductor, which further reduces the volume and weight of system.

II. SOFT SWITCHED DUAL BUCK INVERTER

The dual-buck inverter typically has two buck inverters with one working at the positive half-cycle while the other one operating at the negative half- cycle. The dual-buck type inverters do not need dead time, and they totally eliminate the shoot through concerns, thus leading to greatly enhanced system reliability. The body diode of MOSFET never conducts, and the external diodes can be independently selected to minimize switching losses. However, one of the inherent drawbacks of single dual-buck inverters is the output current zero-crossing distortion. To overcome this disadvantage, new PWM methods need to be introduced. Even though the dual-buck inverters adopt MOSFET devices, they are still the hard-switching VSI. To further reduce the switching loss in power devices and passive filter components, new PWM schemes need to be explored. The circuit diagram of soft switched dual buck inverter with series connected diodes is shown in figure1.

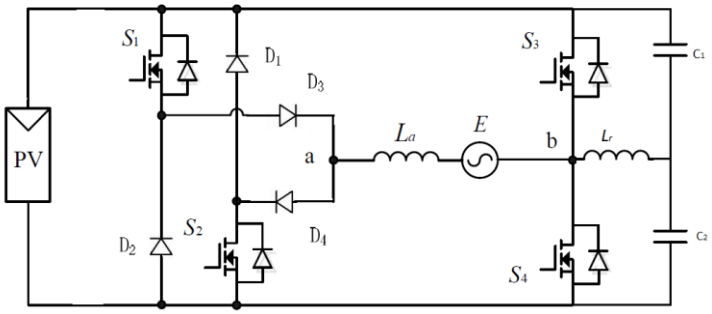

Fig.1. Circuit diagram

A. Modes of Operation:

(a). Mode 1

During positive half period, S1 is modulated in high frequency, while S4 is always ON. When S1 and S4 are on, the current flows through S1, D3, grid and S4 successively. The mode 1 is shown in fig.2.

(b). Mode 2

When S1 is off, the current flows through D2, D3, grid and S4 successively. As shown in Fig. 4, in this freewheeling mode, the diode D4 prevents the current from flowing through the body diode of S2, which avoid the failure of the MOSFET' s reverse recovery. The mode 2 is shown in fig.3.

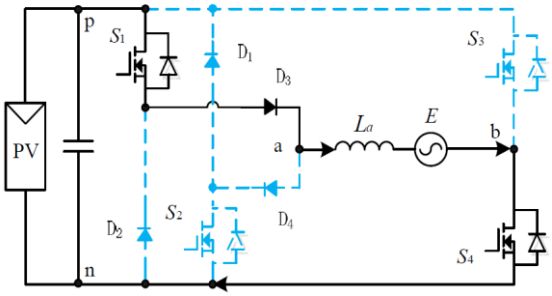

Fig. 2. Mode 1

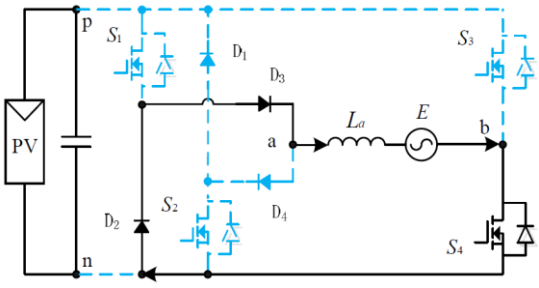

Fig. 3. Mode 2

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(c). Mode 3

During negative half period, S2 is modulated in high frequency, while S3 is always ON. When S2 and S3 are on, the current flows through S3, grid, D4 and S2 successively. The mode 3 is shown in fig.4.

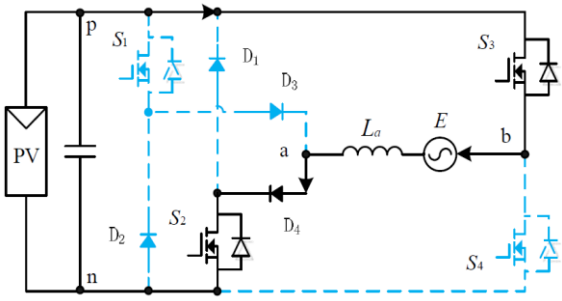

Fig. 4: Mode 3

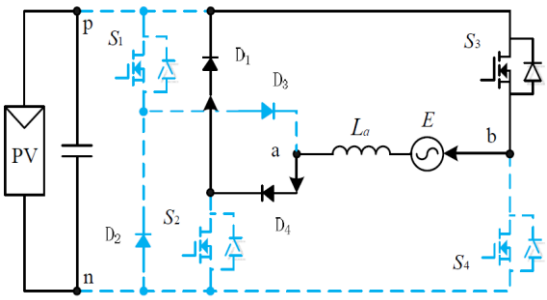

Fig. 5: Mode 4

(d). Mode 4

When S2 is off, the current flows through S3, grid, D4 and D1 successively. As shown in Fig. 6, in this freewheeling mode, the diode D3 prevents the current from flowing through the body diode of S1, which can also avoid the failure of the MOSFET' s reverse recovery. The mode 4 is shown in fig.5.

The control strategy is as shown in fig. 6.

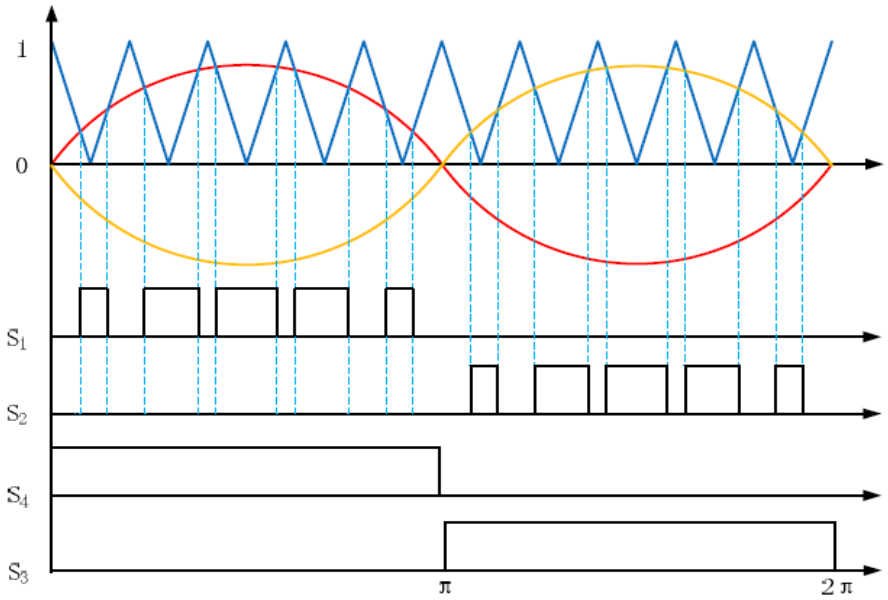

Fig. 6: Control strategy

III. SIMULATION MODEL AND RESULTS

The simulation and experimental results are shown in this section. The proposed inverters in Fig. 4 were simulated in PSIM. The DC voltage is 220V, and the grid voltage is 220V/50Hz. The switching frequency is 10 kHz. The output inductor is 2 mH. The control strategy involves unipolar spwm for switches S_1 and S_2 and simple pwm for switches S_3 and S_4. An input DC voltage of 220 V is applied at the input to obtain an inverter output of 220 V peak.

A. PSIM Model:

The PSIM model of soft switched dual buck inverter is shown in fig. 7.

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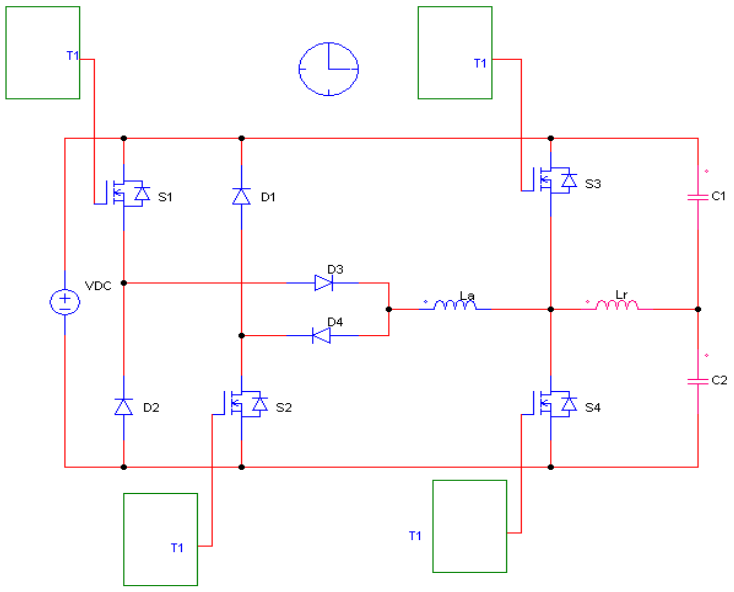

Fig. 7: PSIM model

B. *Simulation Results:*

The input and output voltages obtained are shown in fig. 8 and fig. 9 respectively. An input voltage of 220 V dc is given. The output voltage is obtained as 220 V at its positive and negative peaks.

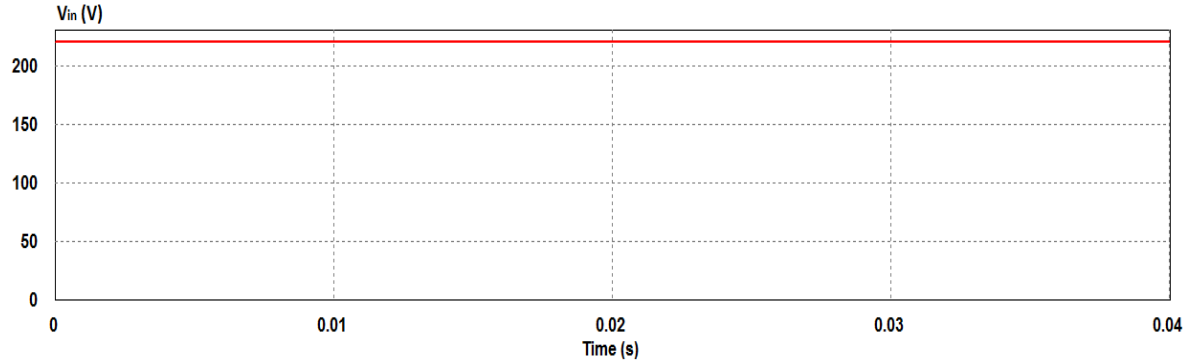

Fig. 8: Input voltage

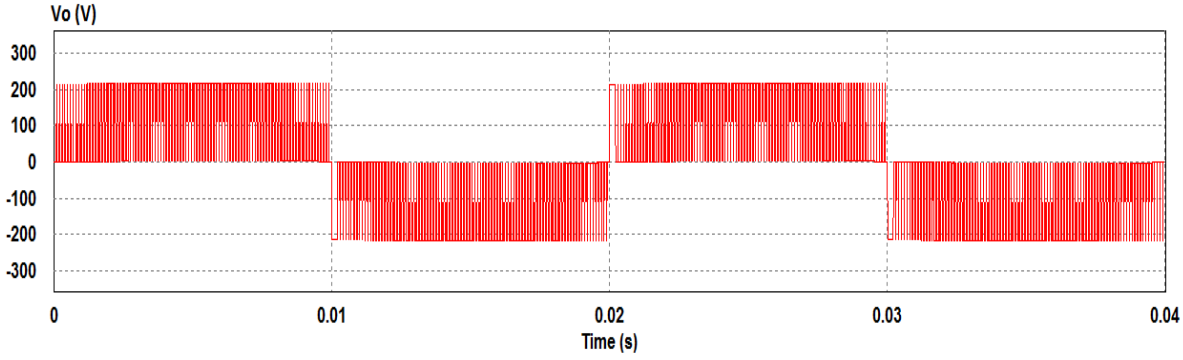

Fig. 9: Onput voltage

The zero voltage switching is obtained for the switches S3 and S4. That is, the turn on of the switch S3 as well as turn off of the switch S4 is under ZVS conditions. The voltage across the switch S4 reaches it's maximum value only with a time delay after the gate pulse. Similarly the voltage across switch S3 is reduced to zero before the gate pulse.

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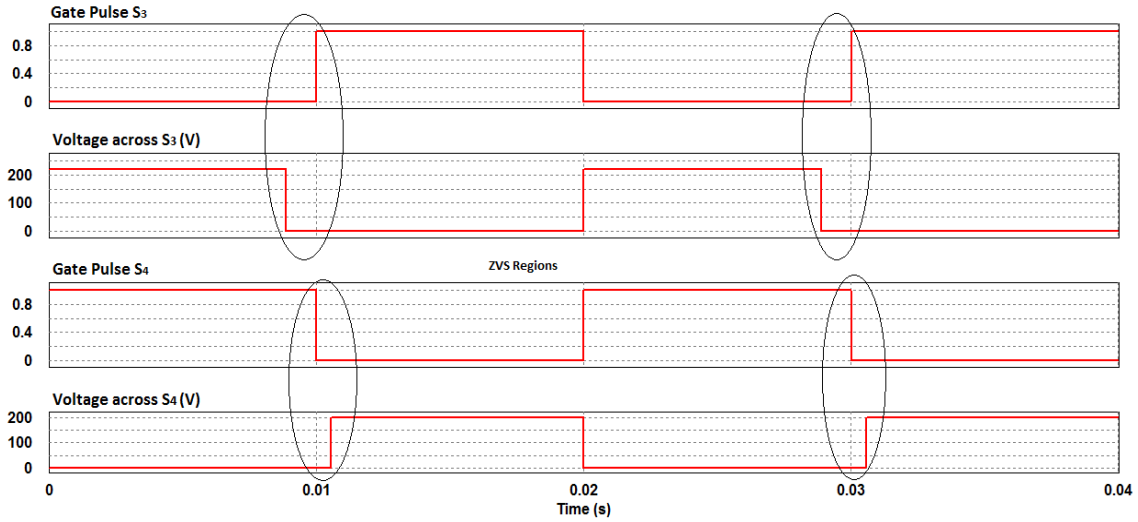

Fig. 10: ZVS property of switches

IV. EXPERIMENTAL SETUP AND RESULTS

A. Experimental Setup:

Hardware setup is done in printed circuit board (PCB) as well as bread board. Control circuit is made in bread board and power circuit in printed circuit board. The implementation of the prototype of dual buck inverter circuit requires two main steps, first is the software implementation. Once the programming is done accurately for generating gate switching for switching devices, the hardware implementation of the circuit can be carried out. Software programming is done in PIC16F877A micro controller.

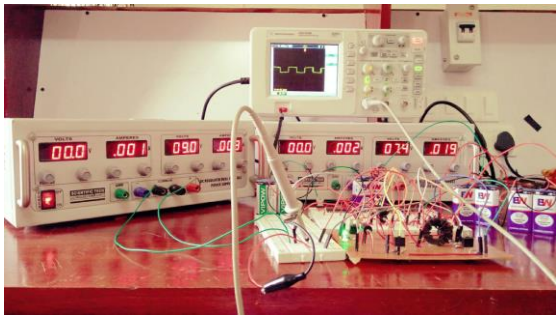

Fig. 11: Experimental setup (front view)

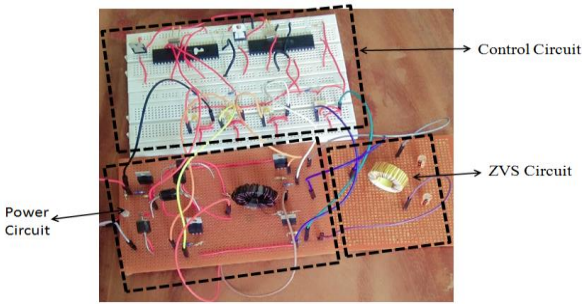

Fig. 12: Experimental setup (top view)

B. *Experimental Results:*

The pulses at output of pic is shown in fig. 13. An inverter output voltage of 5 V is obtained which is shown in figure 14. The prototype is made for an input voltage of 5 V.

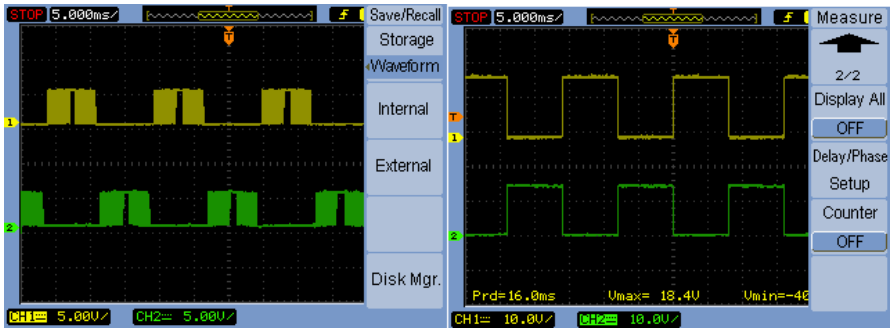

Fig. 13: Pulses at the output of pic

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Port B and port C of pic are used as output for taking pulses. This voltage wont be able to drive the switches in to conduction. There fore driver IC is used which is TLP250. The TLP250 is an optocoupler, which isolates control circuit and power circuit. The input voltage to driver IC should be in the range of 12 V to 30 V. By connecting two 9 V batteries in series an 18 V can be obtained which is provided as input to the TLP250.

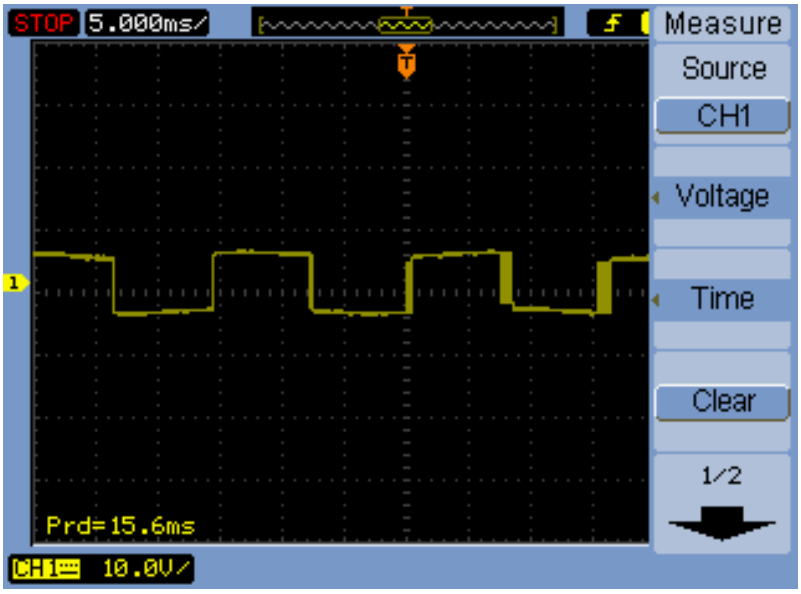

Fig. 14: Output of dual buck inverter

By introducing auxiliary circuit, soft switching property of switches can be obtained. The switch S3 is turned on at zero voltage and the The switch S4 is turned off at zero voltage. The zero voltage switching is shown in fig. 15.

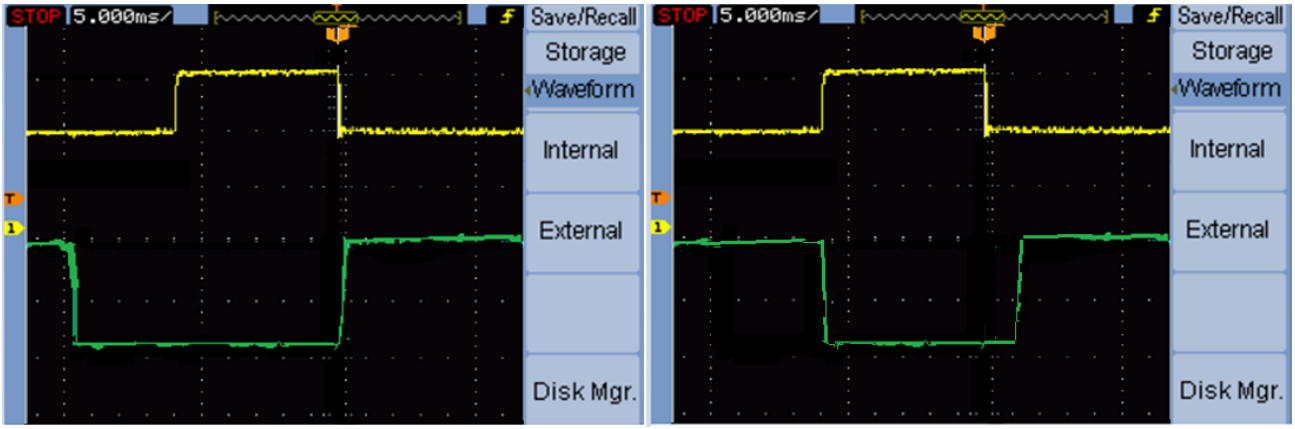

Fig. 15: ZVS property of switches

V. CONCLUSIONS

A soft switched dual buck inverter with series connected diodes is presented in this project. The AC output of the inverter can be connected to the grid system. Compared with other dual buck inverters, the proposed inverter has only one filter inductor. Therefor the volume and weight of the system are observably decreased. Also, the integration is more improved. The voltage dividing capacitor is not needed at the DC side as seen in half bridge style inverter. The voltage stress of power devices can be reduced, which is suitable for the high-voltage and high-power occasions. It retains the advantages of a dual buck inverter as follows: high conversion efficiency, no reverse recovery of body diode. In addition, the switches of the commutation bridge work at power frequency. Thus, the effect of shoot through problem can be ignored. The inverter is verified experimentally for a prototype of 5 V. By providing soft switching techniques, the switching loss during the transitions can be reduced.

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